What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

shallow trench isolation regions formed in trenches provided in the semiconductor substrate;

a pair of source and drain regions formed in the semiconductor substrate, said pair of source and drain regions using a surface of the semiconductor substrate sandwiched therebetween as a channel;

a gate insulating film formed on the semiconductor substrate, in which film thicknesses thereof at a central portion of the channel and at portions contacting with the shallow trench isolation regions are equal; and

a gate electrode formed on the gate insulating film.

2. The semiconductor device according to claim 1,

wherein the gate insulating film includes:

a first insulating film comprised of silicon and nitrogen as main constituent elements thereof; and

a second insulating film formed on the first insulating film, said second insulating film being different from the first insulating film in main constituent elements, and

film thickness of the second insulating film at a central portion of the channel and at portions contacting with the shallow trench isolation regions are equal.

3. The semiconductor device according to claim 1,

wherein the gate insulating film includes;

a first insulating film comprised of silicon and nitrogen as main constituent elements thereof; and

a third insulating film formed under the first insulating film and on the semiconductor substrate, said third insulating film being different from the first insulating film in main constituent elements, and

film thicknesses of the third insulating film at a central portion of the channel and at portions contacting with the shallow trench isolation regions are equal.

4. The semiconductor device according to claim 1,

wherein the gate insulating film includes:

a first insulating film comprised of silicon and nitrogen as main constituent elements thereof;

a second insulating film formed on the first insulating film, said second insulating film being different from the first insulating film in main constituent elements; and

a third insulating film formed under the first insulating film and on the semiconductor substrate, said third insulating film being different from the first insulating film in main constituent elements, and

film thicknesses of the first insulating film, the second insulating film and the third insulating film, respectively, are equal at a central portion of the channel and at portions abutting on the shallow trench isolation regions.

5. The semiconductor device according to any one of claims

2 to 4, wherein the gate electrode is formed on the shallow trench isolation regions without interposition of the first insulating film.

6. The semiconductor device according to any one of claims 1 to 4, wherein a width of a portion of the semiconductor substrate, the portion being sandwiched between the shallow trench isolation regions, is not more than a width of a portion of the gate electrode, the portion being sandwiched between the shallow trench isolation regions.

7. The semiconductor device according to any one of claims 2 to 4, wherein a width of a portion of the semiconductor substrate, the portion being sandwiched between the shallow trench isolation regions is not more than a width of a portion of the first insulating film, the portion being sandwiched between the shallow trench isolation regions.

8. The semiconductor device according to claim 5, wherein a width of the first insulating film in a direction of the channel is equal to a width of the gate electrode in the direction of the channel.

9. The semiconductor device according to claim 5,

wherein the gate electrode contains impurities, and

an impurity concentration of the gate electrode at a portion contacting with the gate insulating film is equal to an impurity concentration thereof at portions contacting with upper planes of the shallow trench isolation regions.

10. The semiconductor device according to claim 5,

wherein the gate electrode is made of polycrystalline silicon containing impurities, and

the gate electrode is a continuous film without interposition of a natural oxide film therein.

11. A semiconductor device comprising:

a semiconductor substrate;

first shallow trench isolation regions formed in trenches provided in the semiconductor substrate;

a first pair of source and drain regions formed in the semiconductor substrate, said first pair of source and drain regions using a surface of the semiconductor substrate sandwiched therebetween as a first channel;

a first gate insulating film formed on the semiconductor substrate, in which film thicknesses thereof at a central portion of the first channel and at portions contacting with the first shallow trench isolation regions are equal;

a first gate electrode formed on the first gate insulating film;

second shallow trench isolation regions formed in trenches provided in the semiconductor substrate;

a second pair of source and drain regions formed in the semiconductor substrate, said second pair of source and drain regions using a surface of the semiconductor substrate sandwiched therebetween as a second channel;

a second gate insulating film formed on the

semiconductor substrate, in which film thicknesses thereof at a central portion of the second channel and at portions contacting with the second shallow trench isolation regions are equal; and

a second gate electrode formed on the second gate insulating film.

12. The semiconductor device according to claim 11,

wherein the first shallow trench isolation regions and the second shallow trench isolation regions have concave portions on upper ends individually thereof, and

depths of the concave portions provided on the first shallow trench isolation regions are smaller than depths of the concave portions provided on the second shallow trench isolation regions.

13. The semiconductor device according to claim 11,

wherein upper surfaces of the first shallow trench isolation regions are formed into convex shapes, and

the second shallow trench isolation regions have concave portions on upper ends thereof.

14. The semiconductor device according to claim 11,

wherein the first gate insulating film includes:

a first insulating film comprised of silicon and nitrogen as main constituent elements thereof;

a second insulating film formed on the first insulating film, said second insulating film being different from the first insulating film in main constituent elements; and

a third insulating film formed under the first insulating film and on the semiconductor substrate, said third insulating film being different from the first insulating film in main constituent elements, and

the second gate insulating film is a silicon oxide film excluding nitrogen as a main constituent element thereof.

15. The semiconductor device according to any one of claims 11 to 14,

wherein the first gate electrode and the second gate electrode are made of polycrystalline silicon films, which are doped with impurities of conductivity types opposite to each other.

16. The semiconductor device according to any one of claims 11 to 14, further including:

a memory section having a plurality of the first gate electrodes; and

a peripheral circuit section having a plurality of the second gate electrodes,

wherein impurities of a first conductivity type are doped in a first number of the first gate electrode out of the plurality of the first gate electrodes,

impurities of a second conductivity type are doped in a second number of the first gate electrodes,

impurities of the first conductivity type are doped in a first number of the second gate electrode out of the plurality of the second gate electrodes, and

impurities of the second conductivity type are doped in a second number of the second gate electrodes.

17. The semiconductor device according to any one of claims 11 to 14, wherein film thickness of the first gate electrode is equal to film thickness of the second gate electrodes.

18. The semiconductor device according to claim 16,

wherein the memory section includes memory transistors and selective transistors,

the peripheral circuit section includes peripheral circuit transistors, and

the selective transistors have constitutions of the gate electrodes and the gate insulating films thereof, the constitutions being identical to constitutions of the gate electrodes and the gate insulating films of any of the memory transistors and the peripheral circuit transistors.

19. A method of fabricating a semiconductor device comprising:

forming a gate insulating film on a semiconductor substrate;

forming trenches in the semiconductor substrate after forming the gate insulating film;

forming shallow trench isolation regions by filling the trenches with insulating materials; and

forming a gate electrode on the gate insulating film and the shallow trench isolation regions.

20. A method of fabricating a semiconductor device

comprising:

forming a first insulating film on a semiconductor substrate;

forming a second insulating film on the first insulating film;

forming trenches in the second insulating film, the first insulating film and the semiconductor substrate;

forming shallow trench isolation regions by filling the trenches with insulating materials;

removing the second insulating film such that the shallow trench isolation regions protrude from an upper surface of the first insulating film; and

forming a gate electrode on the first insulating film exposed and the shallow trench isolation regions.

21. The method of fabricating a semiconductor device according to claim 20, wherein forming a first insulating film is forming a stacked insulating film including a charge storing insulating film capable of storing electric charges.

22. A method of fabricating a semiconductor device comprising:

forming a first gate insulating film on a semiconductor substrate at a memory section and at a peripheral circuit section, said first gate insulating film being comprised of a multilayer film including a silicon nitride film;

forming trenches in the semiconductor substrate at the memory section and the peripheral circuit section after

forming the first gate insulating film;

forming shallow trench isolation regions by filling the trenches with insulating materials;

forming a second gate insulating film at the peripheral circuit section by thermal oxidation after removing the silicon nitride film out of the first gate insulating film at the peripheral circuit section; and

forming a gate electrode on the first gate insulating film, on the second insulating film and on the shallow trench isolation regions at the memory section and at the peripheral circuit section.

23. A method of forming a semiconductor device comprising:

forming a first gate insulating film on a semiconductor substrate at a peripheral circuit section, which includes a high-withstand-voltage transistor region and a low-voltage transistor region, and at a memory section;

removing the first gate insulating film in the low-voltage transistor region of the peripheral circuit section and at the memory section;

forming a second gate insulating film over a surface of all constituents on the semiconductor substrate;

forming trenches in the semiconductor substrate at the memory section and at the peripheral circuit section after forming the second gate insulating film;

forming shallow trench isolation regions by filling the trenches with insulating materials;

forming a low-voltage transistor gate insulating film and a high-withstand-voltage transistor gate insulating film at the peripheral circuit section by thermal oxidation, after removing the silicon nitride film out of the second gate insulating film at the peripheral circuit section; and

forming a gate electrode on the gate insulating film at the memory section, on the low-voltage transistor gate insulating film, on the high-withstand-voltage transistor gate insulating film and on the shallow trench isolation regions.

24. The method of fabricating a semiconductor device according to claim 23,

wherein a plurality of gate electrodes are formed in the memory section and a plurality of gate electrodes are formed in the peripheral circuit section simultaneously while forming a gate electrode, and

after forming a gate electrode, the method further includes:

doping impurities of a first conductivity type into a first number of the gate electrodes at the peripheral circuit section;

doping impurities of a second conductivity type into a second number of the gate electrodes at the peripheral circuit section;

doping impurities of the first conductivity type into the first number of the gate electrodes at the memory section;

and

doping impurities of the second conductivity type into the second number of the gate electrodes at the memory section.

25. A method of fabricating a semiconductor device comprising:

forming a first gate insulating film on a semiconductor substrate at a memory section including a memory cell transistor region and a selective transistor region and at a peripheral circuit section including a low-voltage transistor region and a high-withstand-voltage transistor region;

removing the first gate insulating film in the low-voltage transistor region of the peripheral circuit section and at the memory section;

forming a second gate insulating film comprised of a multilayer film including a silicon nitride film;

forming trenches in the semiconductor substrate at the memory section and at the peripheral circuit section after forming the second gate insulating film;

forming shallow trench isolation regions by filling the trenches with insulating materials;

forming a low-voltage transistor gate insulating film and a high-withstand-voltage transistor gate insulating film at the peripheral circuit section by thermal oxidation, after removing the silicon nitride film out of the second

gate insulating film in the selective transistor region of the memory section and at the peripheral circuit section; and

forming a gate electrode on the gate insulating film in the memory cell transistor region, on the gate insulating film in the selective transistor region, on the low-voltage transistor gate insulating film, on the high-withstand-voltage transistor gate insulating film and on the shallow trench isolation regions.

26. A semiconductor device comprising:

a semiconductor substrate;

an element region of a first conductivity type formed in the semiconductor substrate, said element region having four sides substantially;

a source electrode and a drain electrode formed on two opposing sides of the element region, respectively, said source electrode and said drain electrode being of a conductivity type reverse to the first conductivity type;

a first gate insulating film provided on the element region;

a charge storing region provided on the first gate insulating film, including an insulating film capable of storing data as well as electrically writable and erasable, said charge storing region having two edges on two sides without the source electrode and the drain electrode formed thereon; and

at least one gate electrode provided on the charge storing region, said gate electrode being formed in a manner that distance of two opposing sides without formation of the source electrode and the drain electrode on a lower plane of the gate electrode is made shorter than distance between two edges on the two opposing sides on an upper plane of the charge storing region without formation of the source electrode and the drain electrode.

27. The semiconductor device according to claim 26, wherein the distance of the two opposing sides without formation of the source electrode and the drain electrode on the lower plane of the gate electrode is shorter than the distance between the two edges of the charge storing region by a value in a range from 10 nm to 100 nm.

28. The semiconductor device according to claim 26, wherein the distance between the two edges of the charge storing region is longer than distance of the two opposing sides of the element region without formation of the source electrode and the drain electrode on a plane of the element region facing the first gate insulating film.

29. The semiconductor device according to claim 26, wherein the distance between the two edges of the charge storing region is longer than distance of the two opposing sides of the element region without formation of the source electrode and the drain electrode on a plane of the element region facing the first gate insulating film by a value in a range

from 1 nm to 30 nm.

30. A semiconductor device comprising:

a semiconductor substrate;

an element region of a first conductivity type formed in the semiconductor substrate, said element region having four sides substantially;

a first gate insulating film provided on the element region;

a source electrode and a drain electrode formed in the semiconductor substrate, said source electrode and said drain electrode being of a conductivity type reverse to the first conductivity type;

a charge storing region provided on the first gate insulating film, said charge storing region including: an insulating film capable of storing data as well as electrically writable and erasable; two edges on two opposing sides; and in a state where at least the source electrode and the drain electrode are in a conductive state when a direction of currents flowing on the element region is defined as a first direction and a direction orthogonal to the first direction on the semiconductor substrate is defined as a second direction, two edges in the second direction on an upper plane of the charge storing region;

at least one gate electrode provided on the charge storing region, said gate electrode being formed in a manner that lengths of two sides in the second direction on a lower

plane of the gate electrode are made shorter than distance between the two edges of the charge storing region in the second direction on an upper plane of the charge storing region; and

at least two current terminals connected to the source electrode and the drain electrode, respectively, to detect a state of data storage of the charge storing region depending on any one of a conductive state and an interrupted state between the source electrode and the drain electrode.

31. The semiconductor device according to claim 30, wherein the lengths of the two sides of the gate electrode in the second direction on a plane facing the charge storing region are made shorter than the distance between the two edges of the charge storing region in the second direction by a value in a range from 10 nm to 100 nm.

32. The semiconductor device according to claim 30, wherein the distance between the two edges of the charge storing region in the second direction on a plane facing the first gate insulating film of the element region is made longer than a length of the element region in the second direction.

33. The semiconductor device according to claim 30, wherein distance between the two edges of the charge storing region in the second direction on a plane facing the first gate insulating film of the element region is made longer than a length of the element region in the second direction by a value in a range from 1 nm to 30 nm.

34. A semiconductor device comprising:

a semiconductor substrate;

an element region formed in the semiconductor substrate;

a first gate insulating film provided on the element region;

at least one gate electrode;

an element isolation region formed on the semiconductor substrate, said element isolation region abutting on at least a part of the gate electrode; and

a charge storing region provided on the first gate insulating film, said charge storing region including an insulating film capable of storing data as well as electrically writable and erasable and having an edge positioned in the element isolation region.

35. The semiconductor device according to claim 34, wherein the edge of the charge storing region penetrates into the element isolation region by a value in a range from 0.5 nm to 15 nm.

36. The semiconductor device according to any one of claims 26 to 35, wherein the gate electrode includes:

a lower conductor defined by a rectangular region having two sides substantially parallel to the first direction and two sides substantially parallel to the second direction; and

an upper conductor having any pair of the two opposing

sides substantially parallel to the first direction and the two opposing sides substantially parallel to the second direction of the lower conductor in common, said upper conductor being provided for electrically connecting lower conductors in a plurality of adjacent gate electrodes.

37. The semiconductor device according to any one of claims 26 to 35, further comprising:

a sidewall insulating film formed on a sidewall portion of the gate electrode,

wherein assuming that a face of the sidewall insulating film contacting with the gate electrode is a first side, an edge of the charge storing insulating film facing the gate electrode is formed beyond the first side to a side without formation of the gate electrode.

38. The semiconductor device according to any one of claims 26 to 35, further comprising:

a second gate insulating film provided on the charge storing region,

wherein the gate electrode is formed on the second gate insulating film.

39. A semiconductor device comprising:

a semiconductor substrate;

an element region of a first conductivity type formed on the semiconductor substrate, said element region having four sides substantially;

a first gate insulating film formed on the element

region;

a charge storing region formed on the first gate insulating film, having an insulating film capable of storing data as well as electrically writable and erasable;

at least one gate electrode provided on the charge storing region;

a source electrode and a drain electrode of a conductivity type reverse to the first conductivity type, said electrodes being formed on two opposing sides of the element region, respectively; and

a second gate insulating film disposed between the charge storing region and the gate electrode, said second gate insulating film being formed thicker at a portion of the second gate insulating film under edges of the gate electrode than a portion of the second gate insulating film under a central portion of the gate electrode facing the charge storing region, regarding two sides of the second gate insulating film without formation of the gate electrode and the drain electrode.

40. The semiconductor device according to claim 39, wherein a thickness of the second gate insulating film is formed thicker by a thickness in a range from 0.5 nm to 50 nm at the portion under the edges of the gate electrode than the portion of the second gate insulating film under the central portion of the gate electrode facing the charge storing region, regarding two sides of the second gate insulating

film without formation of the gate electrode and the drain electrode.

41. A semiconductor device comprising:

a semiconductor substrate;

an element region of a first conductivity type formed on the semiconductor substrate, said element region having four sides substantially;

a first gate insulating film provided on the element region;

a charge storing region provided on the first gate insulating film, said charge storing region being comprised of an insulating film capable of storing data as well as writable and erasable and having two edges on two opposing sides;

at least one gate electrode provided on the charge storing region;

a source electrode and a drain electrode of a conductivity type reverse to the first conductivity type, said electrodes being provided in the semiconductor substrate;

current terminals provided in the source electrode and the drain electrode, respectively, for detecting a state of storage of the charge storing region depending on any one of a conductive state and an interrupted state between the source electrode and the drain electrode; and

a second gate insulating film disposed between the

charge storing region and the gate electrode, in a case where a direction of currents flowing at least between the current terminals in a conductive state is defined as a first direction and a direction perpendicular to the first direction on the semiconductor substrate is defined as a second direction, a thickness of portions of the second gate insulating film under edges of the gate electrode in the second direction being thicker than a thickness of the second gate insulating film in the second direction under a central portion of the gate electrode facing the charge storing region.

42. The semiconductor device according to claim 41, wherein a thickness of the second gate insulating film is formed thicker by a thickness in a range from 0.5 nm to 50 nm at the portions under the edges of the gate electrode in the second direction than the portion of the second gate insulating film under the central portion of the gate electrode facing the charge storing region.

43. The semiconductor device according to any one of claims 39 to 42, wherein a thickness of the first gate insulating film is formed thicker at portions under the edges of the gate electrode than a portion of the first gate insulating film under a central portion of the gate electrode facing the charge storing region.

44. The semiconductor device according to any one of claims 39 to 42,

wherein the gate electrode has a stacked conductor region comprised of at least two layers of a lower conductor and an upper conductor in an order from beneath,

the lower conductor is defined by a rectangular region having two sides substantially parallel to the first direction and two sides substantially parallel to the second direction, and

the upper conductor has any pair of the two opposing sides substantially parallel to the first direction and the two opposing sides substantially parallel to the second direction of the lower conductor in common, said upper conductor being provided for electrically connecting a plurality of the adjacent lower conductors.

45. The semiconductor device according to any one of claims 26 to 35, and 39 to 42 further comprising:

an element isolation region disposed adjacently to at least a part of the gate electrode, said element isolation region including an element isolation trench formed by self-alignment with respect to at least any one of the gate electrode, the first gate insulating film, the charge storing insulating film and the second gate insulating film.

46. The semiconductor device according to any one of claims 26 to 35, and 39 to 42,

wherein a plurality of the gate electrodes are disposed on the semiconductor substrate, and

the charge storing layers of the plurality of the gate

electrodes are severed among the gate electrodes adjacent to one another.

47. The semiconductor device according to any one of claims 26 to 35, and 39 to 42, further comprising:

an element isolation region disposed adjacently to at least a part of the first gate electrode, said element isolation region including a high-density impurity region provided in the semiconductor substrate.